A comparative efficiency study on bidirectional grid interface converters applied to low power DC nanogrids

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***Abstract* - This paper describes a comparative efficiency study of different topologies for the bidirectional grid interface converter (BGIC) for applications in DC microgrids, which manage the power flow between the utility grid and the DC microgrid with the intent to regulate the main DC bus voltage and simultaneously ensure grid code compliance at the point of common coupling. In this area a lot of studies emerged to improve renewable energy integration with electrical grid and increase the entire system efficiency. For efficiency analysis, semiconductors and inductors losses were considered based on datasheets information. MOSFETs usage was considered in order to verify the efficiency increasing against IGBTs for BGIC application.**

***Keywords* – DC Microgrids; Bidirectional converter; fullbridge; NPC.**

I. INTRODUCTION

Distributed generation (DG) systems introduce new concepts to the electrical grid, such as microgrids and nanogrids [1]. Nanogrids can be defined as small scale power systems which consist of two or more local power generation, usually based on renewable DG with installed load below 25 kW and limited to a maximum distance of 5 km from the generation sources [2, 3].

Nanogrids are commonly associated with residential and commercial buildings and they can be divided into two categories: ac (alternated current) and dc (direct current). Recent studies estimate that dc systems can improve buildings overall efficiency by 15% to 22%, comparison to ac based systems [4, 5]. This gain mainly occurs due to the elimination of ac-dc power conversion stages in renewable sources and loads.

Figure 1 illustrates a generic dc nanogrid architecture. The main bus interlinks the several power converters which interface distributed generation, energy storage, loads, secondary dc busses and the utility grid, serving as the backbone for the building distribution network. The bidirectional grid interface converter (BGIC) is responsible for the integration of the dc nanogrid and the utility distribution system, managing the power exchange, complying with grid requirements and protecting the nanogrid from grid disturbances. Features such as reliability, high efficiency, reduced volume and weight, and low cost are desirable for the nanogrid interface converters.

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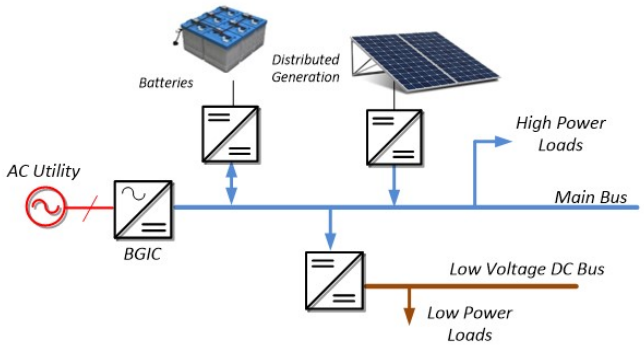

Fig. 1. DC Nanogrid

The BGIC converter must have high efficiency to justify the usage of dc distribution system since this represents the most part of the system total loss [6]. Therefore, the study of the efficiency of different converter topologies suitable for the BGIC implementation becomes relevant, in order to develop a feasible dc nanogrid.

The main goal of the this paper consists in the efficiency study of different single phase ac-dc bidirectional converter topologies applied to the grid interface of a 2 kW dc nanogrid. The topologies Neutral Point Clamped (NPC) and Fullbridge (FB) were considered for the arrange of the single phase ac-dc bidirectional converter. In order to examine the converters efficiency, it was considered that the most significant losses are concentrated at the semiconductors and filter inductors, thus other potential loss sources were disregarded.

The remainder of the paper is organized as follows: Section II presents the considered BGIC structure and the topologies that will be used for the efficiency investigation. Section III discusses the methodology employed in estimating the converter power losses, which rely in datasheet information. Section IV presents the study results and discussions regarding the most efficient converter topology. Section V presents the paper conclusions.

II. GRID INTERFACE CONFIGURATION

The nanogrid grid interface set up considered in this paper is illustrated in Figure 2, which is composed by one ac filter connected to the grid, a two stage Bidirectional Grid Interface Converter (BGIC), and a LC filter linked to the nanogrid main bus.

The nanogrid rated power is 2 kW, and it is coupled to a

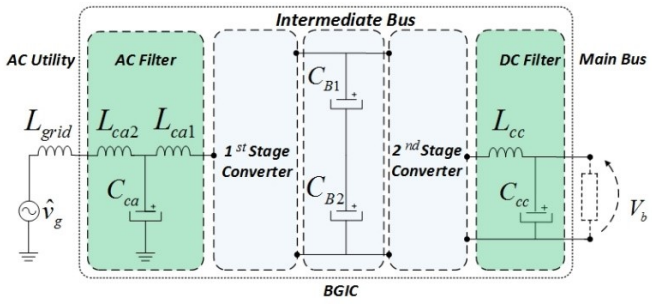

Fig. 2. BGIC Converter

single-phase utility grid, which is the preferred grid connection for microgenerators up to 10 kW [7]. The switching frequency is set in 20 kHz in both converter stages. The nanogrid main bus presents a voltage level of 380V, which according to [3, 5, 8] has shown better outcomes regarding system efficiency and also are being considered for commercial dc distribution standards.

A two stage BGIC provide current limiting capability at both grid and main dc bus sides, enabling the converter to withstand faults in both networks. A higher voltage intermediate bus also allows the reduction of the capacitor bank (C_{B1} and (C_{B2}) [9]. Moreover, the dynamics of the two stages are decoupled, hence the system operation is maintained even under precarious utility grid conditions. The intermediate bus voltage is considered as 600 V and with a 2mF capacitance, which provides a voltage ripple of about 2.5%. The BGIC connection to the utility grid uses a LCL filter, which provides better harmonic component attenuation, allowing inrush current limitation and reduced current ripple in relation to conventional LC filters [10]. At the dc bus side, a LC filter is employed to connect the BGIC second stage and the nanogrid.

A. BGIC Topologies

The converter configuration, presented in Figure 2, consents to disassociate the control loops of both stages [9]. The first stage is responsible for interfacing with the ac utility and the second, with the nanogrid main dc bus, which limits its maximum output current and keeps the voltage at 380 V. This arrangement also permits different converters topologies in its stages, what confers a better project flexibility. The topologies used in the efficiency study for the first stage, fullbridge and NPC, are depicted in Figure 3 and Figure 4 respectively.

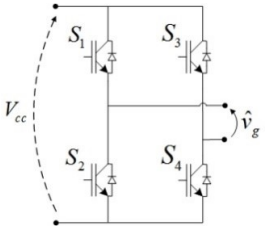

Fig. 3. Fullbridge Converter

The fullbridge arrangement, proposed in [11] to compose the first stage, is traditional, and it has low complexity. Like

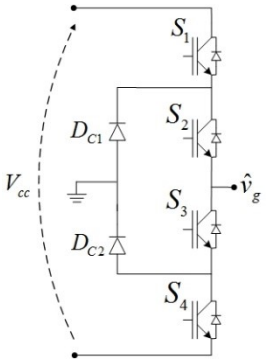

Fig. 4. NPC Converter

the NPC configuration, fullbridge can synthesize three voltage levels [12], with low current THD, which reduces the filter current efforts. The unipolar modulation is considered as the command technique of this converter. The advantage of NPC, cited by industrial applications, is the possibility of using semiconductors designed with half the voltage ratings of the dc bus, whereas for the fullbridge the total bus voltage shall be considered. Therefore, 600 V MOSFETs and IGBTs are suitable for the NPC implementation, whereas only 1200 V IGBTs could be employed in a fullbridge converter, which introduces higher switching losses. Moreover, unlike the fullbrigde, the NPC does not present a common mode voltage between the nanogrid main bus and the utility grounding system, thus no leakage current is generated, increasing nanogrid safety. However, the maximum output voltage of the NPC is only half the one synthesized by the fullbridge, which limits the application of the considered solution to 127 V_{rms} utility grids. For 220V -240V_{rms} systems, the intermediate bus voltage of the NPC converter must be increased. In the second stage, the investigated topologies are the fullbridge, also employed in [12], and the Four Switch Bidirectional dc-dc converter shown in Figure 5.

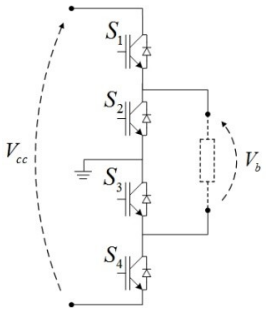

Fig. 5. SNPC Converter

The converter depicted in 5 is a topology derived from a fullbridge NPC converter as described in 6-(a. As the second stage performs a dc-dc conversion, some switches of the NPC topology will be fully on or off, therefore they can be suppressed. Fig. 6-(b shows those switches. In this paper, this topology will be referred as Simplified NPC converter (SNPC).

In the SNPC converter, the switches pair S1-S2 and S3-S4

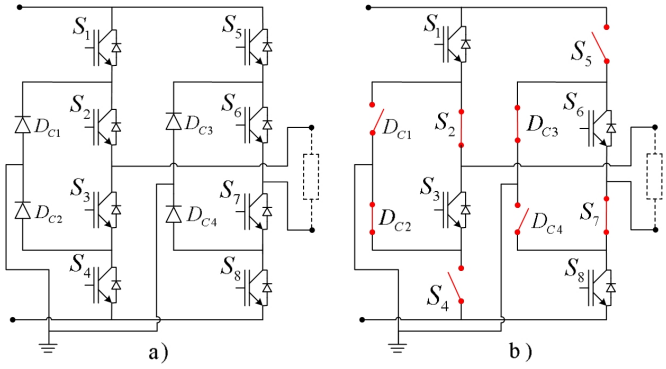

Fig. 6. a) Fullbridge NPC b) Suppressed switches of the NPC)

are complementary. An unipolar PWM is considered for the SNPC, where each switch pair is controlled as a fullbridge converter switching leg would be. Considering that the duty cycle is $-1 \leq D \leq 1$, for $D > 0$, the converter output will switch between 600V and 300 V, and for $D < 0$, it will switch between 300 V and 0V. The converter duty cycle can be calculated by (1)

$$D = \frac{2V_b - V_{cc}}{V_{cc}} \tag{1}$$

Since the nanogrid output voltage under study is 380 V, the SNPC operates with a D higher then 0, as a result the output voltage of this converter would vary between 300 V and 600V, generating a dv/dt of 300 V. Meanwhile, the fullbridge generates a dv/dt of 600 V. As the inductor value depends directly on the voltage derivative [13], its value for SNPC is half of the one considered for the fullbridge topology. As a result, a converter with greater power density can be achieved.

III. POWER LOSSES ESTIMATION

A. Inductor Losses

The power dissipation in inductors are mainly related to two mechanisms: copper losses, due to non-null series resistance, which can vary with the switching frequency and cable proximity; and core magnetic material losses, due to hysteresis, Foucault and residual effects. In a general way, the power dissipated in an inductor winding with distorted current can be estimated by an algebraic sum of the ohmic losses associated with nth-order harmonics, as proposed in [14]. The copper losses are described by (2).

$$P_{copper} = \frac{1}{2} R_{dc} i_{dc}^2 + \frac{1}{2} \sum_{n=1}^{\infty} R_{ac}[n] i_{ac}^2[n] \tag{2}$$

where R_{dc} and R_{ac} consist in winding dc and frequency dependent resistances, respectively; i_{dc} the current average value and i_{ac} the rms value of the alternating component R_{dc} is calculated from physical parameters and wire resistivity, and R_{ac} is computed from skin and proximity effects. As skin and proximity effects in the considered switching frequency are very small, in this, the inductors wire resistance will be considered equal to R_{dc}. In contrast, the mean core losses are estimated from [15, 16], which represents an optimization from what is proposed in [17].

B. SEMICONDUCTOR LOSSES

The calculation of semiconductor losses is done through the Thermal Module tool embedded in PSIM software. This tool provides a fast and simple way to estimate semiconductors conduction and switching losses (Diodes, IGBTs and MOSFETs) during the converter simulation. The Thermal Module tool allows the insertion of curves and data informed by the semiconductors datasheet, which results in very good estimation of real semiconductor losses. In the case of diodes and IGBTs, the user can add curves for different operating temperatures, which allows the thermal simulation to incorporate the influence of the thermal circuit on the semiconductor losses. For MOSFETs, however, only a few data points are inserted, therefore, the model does not consider the influence of temperature variation, resulting in very conservative estimations. In this paper, in order to obtain a more accurate estimation of power MOSFETs losses, the information displayed in the datasheet were used to compile I_{DS} x V_{DS}, I_{DS} x E_{on} and I_{DS} x E_{off} curves for different temperature and gating conditions, mimicking the data available for IGBTs. These curves were later include in an IGBT Thermal Model, which presents a better temperature dependent simulation. The main obstacle in building such curves are associated with the MOSFET input capacitance non-linearity during turn-on and turn-off. Therefore, it was necessary to resort to the techniques described in [18, 19] in order to perform the required numerical calculations.

IV. RESULTS

The BGIC efficiency calculation considered the semiconductor losses estimated by PSIM during the simulation of each converter configuration and the inductor losses, calculated separately through the inductor currents provided by the simulations. In the NPC topology, the impact of the utilization of CoolMOS devices over conventional IGBT in the converter efficiency was also assessed. The electrical characteristics of the 2kW nanogrid and components values used during simulation are presented in Table I.

TABLE I
Electrical characteristics of the nanogrid

Variable	Value
f_{sw}	20 kHz
V_{cc}	600 V
V_b	380 V
v_g	127 V_{rms}
L_{ca1}	600 μH
L_{ca2}	200 μH
C_{ca}	16 μF
L_{cc}	3.7 mH
C_{cc}	100 μF
C_{B1-B2}	2 mF

A. Fist Stage Semiconductor Losses

The semiconductors used in the first and second stages, for NPC, FB, and SNPC are presented in Table II. As in the NPC topology each switch will be submitted to a voltage level of 300 V, half the intermediate bus voltage, 600V MOSFET and IGBT were considered for the NPC simulations. In the other

hand, for the FB topology, 1200V IGBT were used, since this converter applies the whole intermediate bus voltage on the power switches.

TABLE II
Semiconductors used in each converter

Converter	Semiconductor	
1^{st}Stage-Fullbridge	IRG7PH46UDPbF (1200V IGBT)	
1^{st}Stage-NPC IGBT	IKW50N65H5 (1200V IGBT)	IDW30E65D1 (600V Diode)
1^{st}Stage-NPC Mosfet	IP260R045CP (600V Mosfet)	IDW30E65D1 (600V Diode)
2^{nd}Stage-Fullbridge	SK25GH12T4 (1200V IGBT)	
2^{nd}Stage-Fullbridge	SK30GBB066T (600V Mosfet)	

In order to evaluate the worst case scenario, regarding the converter efficiency, all simulations assumed a semiconductor junction temperature of 150^{o}C. Figure 7 presents the total calculated losses for all three BGIC first stage topologies, assuming a switching frequency of 20 kHz and an injection of 2 kW in an 127 V_{rms} single-phase utility grid.

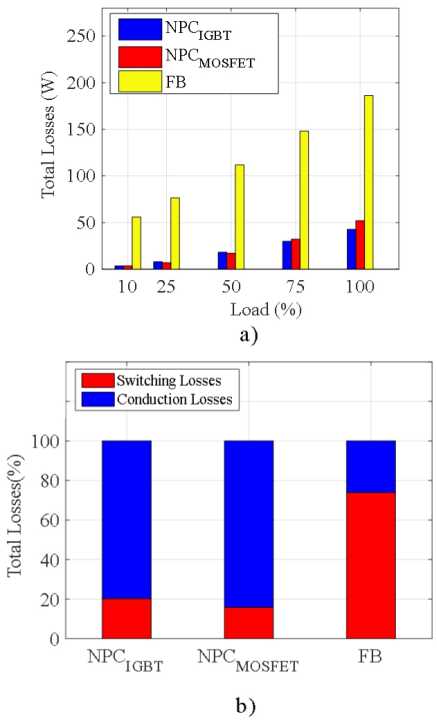

Fig. 7. Losses for Fullbridge, NPC with IGBT and NPC with MOSFET converters in the first stage: a) Total losses b) Percentage losses.

According Fig.7-a), e.g., in a full load situation, the FB converter dissipates approximately 180 W, which is about 4 times more power than the NPC topologies. It can also be observed that for lower output powers the disparity between topologies is accentuated. Regarding the comparison between the utilization of MOSFETs and IGBTs in the NPC topology, also in full load, the MOSFET NPC dissipated 4 W more power than the IGBT NPC. This small difference suggests that, for the used semiconductors, a topology with IGBTs can provide about 10% less losses than a MOSFET NPC. Fig.7-b) shows the percentage loss ratio for 100% load. It can be noticed that 73% of the FB converter semiconductor losses are related to switching losses, whereas the IGBT NPC presents 20% of switching losses and the MOSFET NPC, 16%. This loss distribution was expected, since devices with higher voltage blocking capability, such as the ones employed in the FB converter, tend to present slower transition times, which increases switching losses. On the other hand, for the same operating conditions MOSFETs present lower switching losses and higher conduction losses than IGBTs, as was indicated by the NPC simulation. As a conclusion, it can be said that the excessive switching losses presented by the FB topology can significantly affect the overall efficiency of the grid interface converter, compromising the benefits of employing a dc power distribution in residential and commercial buildings. Therefore, multilevel topologies as the NPC are more suitable for such application. Moreover, for the current silicon based device technology, the utilization of CoolMOS showed no improvement in the converter efficiency in relation to IGBT devices.

B. Second Stage Semiconductor Losses

For the topologies presented for the second stage, it is considered only IGBTs for SNPC, since the previous results showed that the losses generated by 600V MOSFETs and IGBTs has similar values. Fig.8 illustrates the derived losses from second stage converters. According to the BGIC converter section, it is possible to use an inductor in the SNPC with half of calculated value for FullBridge. Nevertheless, it is selected the same inductor for both topologies in the simulation in order to calculate the losses.

The FB converter dissipates about 83 W against 53 W of SNPC in full load. At the same load condition, 86% of the FB topology losses are related to switching losses, whereas in the SNPC, the switching losses represents 80% of the total power dissipation, as can be seen in Fig.8-(b. Although the observed distribution of losses is similar to both converters, the magnitude of the power dissipation is higher for the FB topology. Another behavior that can be observed is that for lower output powers, the difference between topology losses is reduced, notwithstanding, the SNPC shows better efficiency than the FB in all evaluated situations.

C. Inductors

The filter inductors of the BGIC are designed considering iron powder cores from the high flux family, manufactured by Magnetics [20]. Table III presents the inductors design parameters for the regarding the criteria suggested in [20].

Table IV shows the losses derived from the inductor of the first stage . In a general manner, the losses are too small when compared to the total power delivered to the load. The maximum obtained value is 1.77% for 10% load and minimum of 0.20% for 100% load, noting that the most significant part of those losses is related to core losses.

According to [20], in order to evaluate the design of the inductor core, it is necessary to verify its temperature increase.

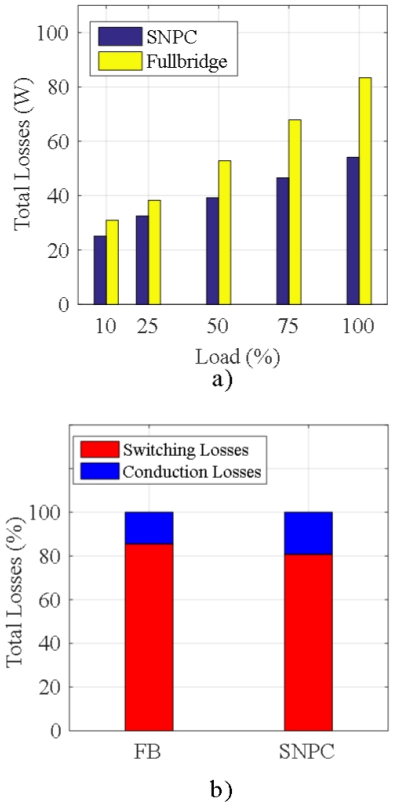

Fig. 8. Losses for Fullbridge and SNPC converters in the second stage: (a) Total losses (b) Percentage losses

TABLE III
Semiconductors used in each converter

Parameter	L_{ca1}	L_{ca2}	L_{cc}
Inductance(μH)	600	200	3700
Number of series units	1	1	1
Number of turns	74	33	183
Number of wires per turn	14	14	3
Wire gauge (AWG)	19	19	19
Core Model(Magnetics)	58099	58617	58110
Relative Permeability	60	60	60
Resistence (Ω)	0.014	0.005	0.081
Fill factor (%)	26.7	31	35.70
Overall volume(m^3)	0.007	0.002	0.0037

TABLE IV
First stage inductors losses

Load	**Total**		**Copper**	**Core**	**Temperature Inc.**	
(%)	(W)	(%)	(W)	(W)	(^{o}C)$_{L_{ca1}}$	(^{o}C)$_{L_{ca2}}$
10	3.51	1.77	0.002	3.51	6.66	0.01
25	4.29	0.86	0.011	4.28	7.86	0.08
50	4.67	0.47	0.045	4.63	8.39	0.26
75	4.99	0.33	0.101	4.89	8.78	0.52
100	5.42	0.27	0.180	5.24	9.31	0.84

The same author describes the procedure for calculating this temperature rise, thus, this is omitted here. A maximum core operating temperature of 100^oC is considered as the design criterion, and the room temperature at which the device is located is 45^oC. The maximum temperature increase of 9.31^oC ensures that the device does not reach the limit considered in the design and makes it feasible to be used. For the second stage, the losses in the inductor presented in Table V also suggest a low significance against the converter total power, e.g., about 0.47% losses for 100% load. The core losses are still superior to copper losses as well as in the first stage, however, for the second stage the conduction losses represent about a quarter of the total losses while in the first stage the conduction losses are practically disregarded.

TABLE V
Second stage inductor losses

Load	**Total**		**Copper**	**Core**	**Temperature Inc.**
(%)	(W)	(%)	(W)	(W)	(^{o}C)$_{L_{cc}}$
10	6.96	3.48	0.02	6.94	27.5
25	7.11	1.42	0.14	6.97	28
50	7.59	0.75	0.5	7.03	29.6
75	8.35	0.55	1.26	7.09	32.1
100	9.4	0.47	2.24	7.15	35.4

Knowing that the losses in the inductors are related to the voltage integral between their terminals (Magnetic Field) [15, 16], it is understood that the losses developed in the inductor for SNPC and FB are different, but the meaningfulness of those losses in relation to the converter output power is still very small as shown in Table V (0.47% for 100% of the load). Therefore, considering the worst case scenario, the inductor losses obtained with the FB topology were assumed for the remainder of this study. Considering the inductor operating temperature criterion, the maximum temperature rise of 35.4^oC credits the possibility of using the inductor since it reaches a maximum temperature of 80.4^oC.

D. Global Efficiency

From the data described in Tables IV, V, and the converters losses, it is possible to account for the global efficiency of the BGIC different possible configurations. The obtained results are shows in VI.

TABLE VI
Total Efficiency

1^{st} **Stage**	2^{nd} **Stage**	**Efficiency(%)**
Fullbridge	Fullbridge	86.20
Fullbridge	SNPC	87.57
NPC Mosfet	Fullbridge	93.65
NPC Mosfet	SNPC	94.51
NPC IGBT	Fullbridge	93.51
NPC IGBT	SNPC	94.96

The use of NPC in the first stage presents a considerable gain in converter efficiency independently of the second stage topology. The configuration that presented the best efficiency is the NPC with IGBT in the first stage and SNPC in the second stage, reaching approximately 95% efficiency. Whereas the worst case scenario, 86.2%, is achieved with the use of the FB topology in both stages. The overall efficiency achieved with first stage in NPC, for MOSFET and IGBT, is nearly the same. It suggests that, considering the current generation of silicon devices and under the same voltage and current requirements, the power switch model has little influence on the converter efficiency. Further improvements, however, can be expected

with the employment of different device technologies, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), which present very small switching losses [6].

V. CONCLUSIONS

This work presented an efficiency study comparing the performance of different converter topologies for the implementation of a two-stage bidirectional grid interface converter applied to a 2kW dc nanogrid. The Thermal Module tool of the software PSIM was used to survey the losses of the semiconductors used in the topologies, which is based on the devices characteristic curves available in the datasheets, and represents a fast, simple and accurate method to estimate losses. The losses in the inductors were raised from a numerical calculation proposed in [18] as a function of the physical parameters of the core and the voltage between the inductor terminals. The study has showed that inductor losses are relatively small, compared to the converter output power, presenting percentage losses of 0.27% and 0.47% for the converter first and second stage, respectively. The highest efficiency scenario is achieved with the first stage composed by a NPC topology and second with a SNPC, approximately 95% This second stage topology were derived from a fullbridge NPC structure, considering that for dc-dc operation some switches are inoperative. It is also observed that, for the chosen semiconductors, it is not possible to verify a considerable difference in the losses for use of MOSFET or IGBT in the NPC topology.

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