Distributed Secondary Level Control for Energy Storage Management in DC Microgrids

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***Abstract*—DC microgrids have been known to be a promising solution for improving renewable energy integration with electrical grid and enhancing the system's overall energy efficiency. A key component of this microgrid is the energy storage system, which besides smoothing the intermittent behavior of renewable sources, also allows intentional islanding and the execution of optimization routines to improve the microgrid performance. Assuming that storage systems in commercial and residential buildings will mostly be composed of multiple storage units, an energy storage management system, which provides charge/discharge monitoring and state-of-charge (SOC) equalization, is needed to prevent overcharging the units or their uneven use, which can lead to faster deterioration of battery banks. This paper proposes an energy storage management system based on distributed secondary level control, which promotes charge/discharge control and provides SOC equalization simultaneously. The SOC imbalance compensation alters the energy storage unit virtual droop resistance according to the difference between the unit SOC and the microgrid average SOC, thus the compensation intensity is dependent on the imbalance level being suitable to be employed in dc bus signaling controlled microgrids.**

***Index Terms*—DC microgrids, dc bus signaling, distributed energy storage units, energy management, hierarchical control.**

I. Introduction

DIRECT current microgrids have become a subject of intense studies in recent years, since they provide a simpler and more efficient way for integrating intermittent renewable energy sources (RES), storage devices and loads, especially in residential and commercial buildings [1]–[9]. Although shifting from an AC-based distribution system to DC distribution requires a considerable amount of investment and development, the perspectives for increasing the overall building energy efficiency in about 10% to 28% [10], [11], due to the mitigation of reactive power and harmonic issues along with the reduction in the set of power conversion stages needed to interconnect distributed RES, storage devices and loads, are a significant driving force which is pushing companies and researchers worldwide into solving technical problems and assuring the DC microgrid feasibility.

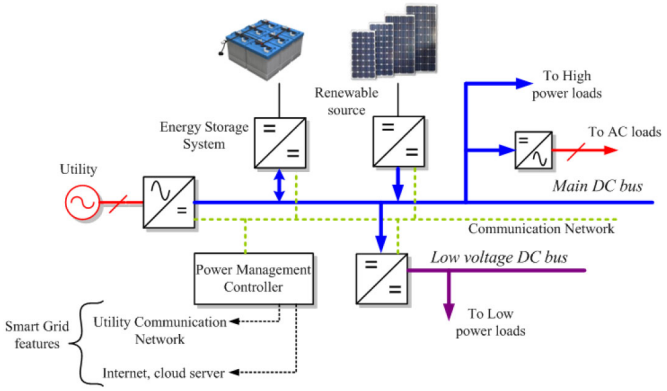

Fig. 1. DC microgrid architecture for residential and commercial applications.

The architecture of a DC microgrid for commercial and residential buildings applications is presented in Figure 1. The system backbone is a main DC bus, in the 300V to 400V voltage range, which interconnects sources and high power loads. This main bus can be derived into several low voltage busses (12V-48V) to supply low power loads, e.g., consumer electronics and room lighting, and provide a safer environment for the human occupants of buildings [1]. AC subsystems can also be considered to supply loads which are not compatible with DC. Power electronic converters are employed as the interface between sources and loads and the microgrid DC busses. A key component of this architecture is the energy storage system (ESS) which, besides smoothing the intermittent behavior of RES, allows the microgrid to island itself from the utility grid during a fault or a severe disturbance, ensuring the local network a higher power quality and also enabling the implementation of energy management strategies which can optimize the power consumption of the microgrid and improve the lifetime of the many system elements.

Assuming that the building power demand can increase over time, the microgrid capacity should enlarge accordingly, hence the microgrid architecture needs to be flexible enough to accommodate an enhancement in power generation and storage capacity not always provided with the same technology employed in the original design. Therefore, it can be expected

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that the microgrid in most buildings will be composed by multiple RES power generation units (PGU) and energy storage units (ESU) distributed throughout the facility, thus the microgrid control scheme must accomplish proper PGU and ESU power sharing and energy storage management alongside with the main DC bus voltage control in order to achieve voltage stability and optimal performance. There is a vast literature addressing DC power systems control [3], [12]–[18], mostly based on decentralized voltage droop control. However, in a microgrid, where the operating conditions of each power source are altered by the system load and environmental aspects, some power management process is required to provide a suitable power flow. Centralized control is a possibility [3], however, the dependency on the communication network can compromise the system robustness and resilience. Distributed power management based on voltage bus variations, as DC bus signaling (DBS) [1], [15], [16], associates simplicity and robustness to the microgrid architecture. The performance of a DBS controlled microgrid can also be optimized through the employment of hierarchical layers of control [13], [18], a communication network will be involved, a failure on it will interfere with the system performance but not necessarily preclude its operation.

In most microgrids, the energy storage system is treated as a single unit, for control purposes, however, as aforementioned, it is more likely that the ESS will be constituted by multiple ESU, hence, the microgrid operation can lead to inadequate situations, as overcharge and state-of-charge (SOC) imbalance. In some circumstances, the employment of an energy storage management system is relevant, which will be responsible for monitoring the ESU charge/discharge conditions, thus avoiding hazards to the battery cells and equalizing the SOC inside the ESU and among different units. The ESU converter control loops, if properly designed, can manage the first assignment easily. The SOC equalization inside an ESU is usually performed by a battery management system (BMS) [19], [20], the balance among different ESU, however, is promoted by the adaptation of the ESU converters controllers [19]–[22]. The BMS can work unaware of the microgrid operation or in cooperation with it, but this system is not the focus of this paper, therefore, it will be assumed for further discussions that each storage device in an ESU presents the same SOC. Regarding the equalization among different ESU, in [19] and [20] the droop resistance (R_D) of the ESU converter is adjusted according to its respective SOC and power flow, $R_D \propto 1/SOC^n$ during discharge and $R_D \propto SOC^n$ in charge mode, where n is a convergence factor. The higher the n, the faster the SOC imbalance is reduced, however, voltage deviation is dramatically degraded. In [21], a Fuzzy Interference System is employed to establish the relationship between the droop resistance and SOC, good balance and voltage deviation is achieved but a drawback is the complexity of the controller design. The use of higher hierarchical levels to manage the SOC imbalance and other power management functions of a DC microgrid have been exploit in some publications as well [23], [24]. Multiple goals can be reached in this manner, but the dependency on the communication network can produce a single point of failure.

The association of SOC balancing algorithms and DC bus signaling control of DC microgrid have not yet been described in the literature and most distributed methods rely on very small voltage deviation to reach the equalization goal, thus their application to DBS power management is restricted. The use of higher control hierarchy to promote SOC balance is quite interesting, however the algorithm must account for communication failures and not compromise the ESU operation due to those failures. This paper will focus on the energy storage management of energy storage units, proposing a control method, based on distributed secondary control, that achieves charge/discharge monitoring and SOC balancing simultaneously. During SOC equalization ESS droop resistance will be modified according to the imbalance level, therefore the interference with the DBS voltage deviation design will be weighted by the total SOC imbalance and will gradually be decreased as SOC evens over time. A secondary layer controller will be employed to compute the ESS average state-of-charge and a low bandwidth communication link will be in charge of the information exchange. The system performance will be experimentally verified in a 2kW scaled DC microgrid.

Section II will describe the proposed control method and SOC compensation algorithm. The influence of SOC balancing in the system stability will also be evaluated. Section III presents simulation results to assess the energy storage management method over different conditions. Section IV will present the experimental validation of the system operation and Section V will provide the paper conclusions.

II. Energy Storage Unit Control Method

The architecture of the energy storage system considered in this paper comprises a set of energy storage units, each one composed by a bidirectional boost converter and a battery string of fourteen Lead-acid accumulators of 40Ah nominal capacity, as depicted in Figure 2, for a two unit storage system. The remainder of the microgrid sources are aggregated in a Thevenin equivalent voltage source for study purposes. The system can operate in stand-alone mode, where only the ESS is responsible for regulating the microgrid main DC bus or in connected mode, where the equivalent source aids the ESS in voltage regulation. The proposed control diagram used in each ESU is depicted in Figure 3.

A. Charge/Discharge Control

The control system assumes that the microgrid employs a DC bus signaling power management strategy, thus it relies on the variation of the DC bus voltage level to determine and regulate each ESU power flow. From the microgrid perspective, it is desirable that the ESU behaves as a droop controlled voltage source, which is compatible with the DBS design, however, in order for this control approach to comply with battery manufacturer's charging specifications, as maximum charge current and voltage, the droop resistance must be constantly modified. A solution for this situation, which is considered in this paper, was introduced by the authors in [25], where two distinct converter voltage control loops are employed, one for regulating the power flow between the ESU and the microgrid

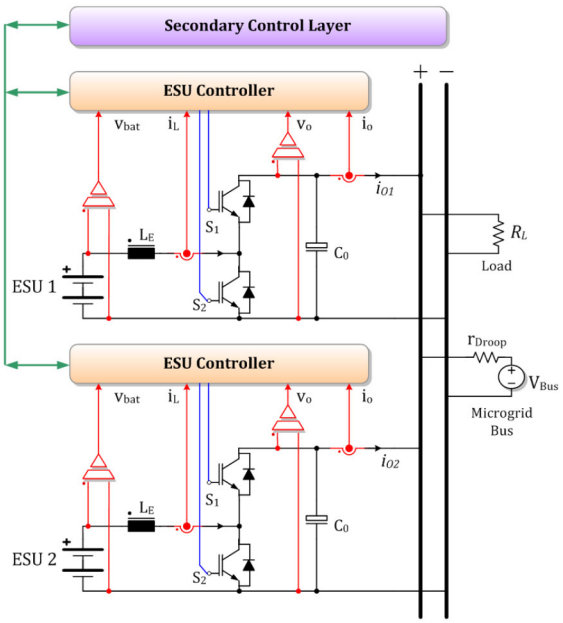

Fig. 2. Energy Storage System architecture.

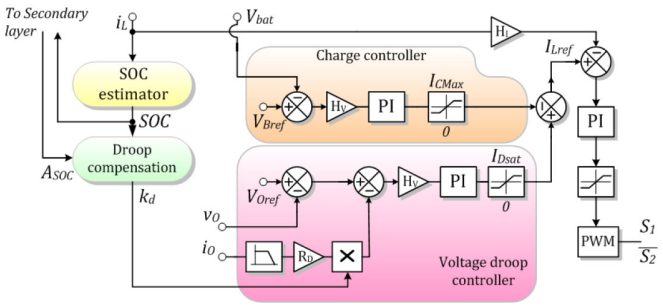

Fig. 3. ESU control diagram.

bus, called Voltage Droop Controller, and other for controlling battery charging, named Charge Controller. The Voltage Droop Controller attempts to regulate the microgrid DC bus (V_O) to a level defined in (1), where V_{Oref} is the bus voltage reference at no load, R_D is the droop resistance, i_O is the converter output current and k_d is a compensation factor used for SOC balancing. As the actual bus voltage depends on other sources and loads as well, this controller will determine the flow direction of the converter output current i_O. The Charge Controller aims to regulate the battery bank terminal voltage to V_{Bref}, which represents a desired charge voltage, e.g., fluctuation or equalization voltages. The current reference for the inner control loop is defined as (2), i.e., the difference between the output of the Voltage Droop Controller (i_{droop}) and the Charge Controller (i_{charge}).

$$V_O = V_{Oref} - R_D \cdot k_d \cdot i_O \tag{1}$$

$$i_{Lref} = i_{droop} - i_{charge} \tag{2}$$

It can be noticed that both voltage loops are competing for the boost inductor current control, therefore the range of influence of each loop must be limited, in order to provide a predictable behavior for this control strategy. This is accomplished through the saturation levels of the PI controllers,

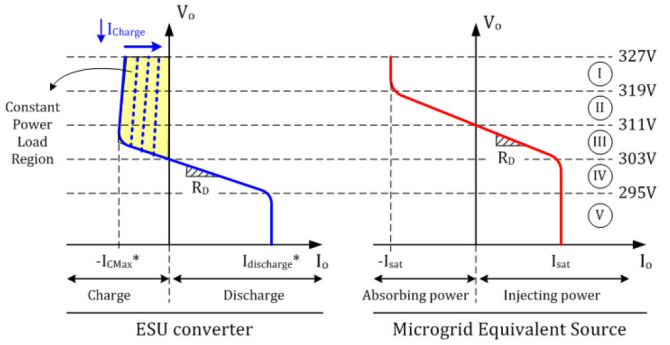

Fig. 4. ESU converter output static characteristic.

which limits i_{droop} and i_{charge} between zero and a maximum level. As seen in Figure 3, the maximum value for i_{charge} is I_{CMax}, which represents the maximum charge current for the battery bank and i_{droop} is limited to I_{Dsat}, which defines the maximum battery discharge current. Actually $I_{Dsat} = I_{CMax} + I_{discharge}$, where $I_{discharge}$ is the maximum discharge current. This means that when the microgrid requires power from the ESU, the Voltage Droop Controller can overcome the Charge Controller output and take control of the converter inductor current and whether the microgrid produced power is high enough the Charge Controller will assume. The correspondent VxI static characteristic of the ESU converter output is shown in Figure 4, along with the considered behavior of the microgrid aggregated voltage source. I^*_{CMax} and $I^*_{discharge}$ refers to the inductor current limits reflected to the converter output. It can be considered that the system will operate in sectors III and IV.

The Voltage Droop Controller will be mostly responsible for the ESU dynamics, since battery charging is a very slow process, which will keep i_{charge} practically constant for a very long period of time. Therefore, the ESU will behave as a droop controlled voltage source in most situations and as a constant power load (CPL) if the microgrid available power is higher than the ESS charge power. As i_{charge} tends to be reduced as the battery bank becomes fully charged, the converter negative current limit will decrease accordingly.

B. State-of-Charge Balancing

In order to promote SOC equalization, the power which each ESU absorbs or supplies the microgrid must be weighted regarding its state-of-charge, e.g., the ESU with higher available charge must supply more power and absorb less power than the other units in the energy storage system. This compensation can be achieved in a distributed manner by modifying the droop resistance value of the Voltage Droop Controller, through the compensation factor k_d. Obviously, this compensation will reduce the ESS equivalent droop resistance, thus interfering with the DBS operation, since maximum voltage deviation is reduced as well. Therefore, it is desirable that modifications on the ESS equivalent droop resistance occurs only when necessary. This however, cannot be accomplished solely with local ESU information, since each ESU must be aware of other units SOC to decide whether droop resistance

compensation is required. In this paper, the compensation algorithm uses a secondary level controller to establish the ESS average state-of-charge (A_{SOC}). Each ESU estimates its own SOC, through (3), where j is an ESU identifier index, SOC_j^0 is the ESU initial SOC and C_{Bat} is the battery bank rated capacity, and informs it to the secondary controller, the A_{SOC} is then computed, as an arithmetic average, and passed on to the ESU. The local droop compensation will calculate k_d according to (4), where $p \geq 0$ is a factor used for convergence. A low bandwidth communication link is employed for the information exchange between the ESU and secondary layer. In case of communication failure, the ESU controller will disable the SOC balancing droop compensation, in order to prevent ESS operation disruption.

$$SOC_j = SOC_j^0 - \frac{1}{C_{Bat}} \int i_{Lj} dt \tag{3}$$

$$k_{dj} = \begin{cases} exp\left[-p \cdot \left(SOC_j - A_{SOC}\right)\right], & \text{if } i_O > 0 \\ exp\left[p \cdot \left(SOC_j - A_{SOC}\right)\right], & \text{if } i_O < 0 \end{cases} \tag{4}$$

Analyzing the compensation factor described in (4) more closely, it can be noticed that the algorithm will exhibit two distinct behaviors: one during ESU discharge ($i_O > 0$) and another during charge mode ($i_O < 0$). In the first situation, if an ESU possesses an instantaneous SOC greater than the ESS average, i.e., $SOC_j - A_{SOC} > 0$, it will lead to $k_{dj} < 1$, meaning that the ESU droop resistance will be lowered and the unit will provide more power to the microgrid than it would do without the compensation influence. On the other hand, if $SOC_j - A_{SOC} < 0$, the compensation factor will be greater than 1, increasing droop resistance and reducing the unit delivered power. In charge mode, the behavior will be exactly the opposite. Consequently this compensation algorithm tends to gradually equalize the storage units state-of-charge either in charge or discharge mode. It is important to notice that the compensation algorithm will only actuate when there is a SOC imbalance among the ESU, once the stored charge is equalized, k_{dj} will converge to 1, returning droop resistance to its original value and restoring DBS normal operation. An exponential function was chosen to describe the $k_{dj} - SOC_j$ relationship, since it enforces more significant droop resistances differences among ESU for a given SOC imbalance than linear or low order polynomial functions, hence promoting faster SOC equalization. As it will be clear later, the convergence factor p is an dimensionless parameter which adjusts the speed of SOC equalization.

The DC bus voltage can be calculated, in stand-alone mode, as (5), where R_L is the load resistance and R_{Deq} is the ESS equivalent droop resistance, defined as (6).

$$V_O = V_{Oref} \cdot \frac{R_L}{R_L + R_{Deq}} \tag{5}$$

$$\frac{1}{R_{Deq}} = \sum_{j=1}^{n} \frac{1}{R_{Dj} \cdot k_{dj}} \tag{6}$$

The ESU output current is defined as (7).

$$I_j = \frac{V_{Oref} - V_O}{R_D \cdot k_{dj}} \tag{7}$$

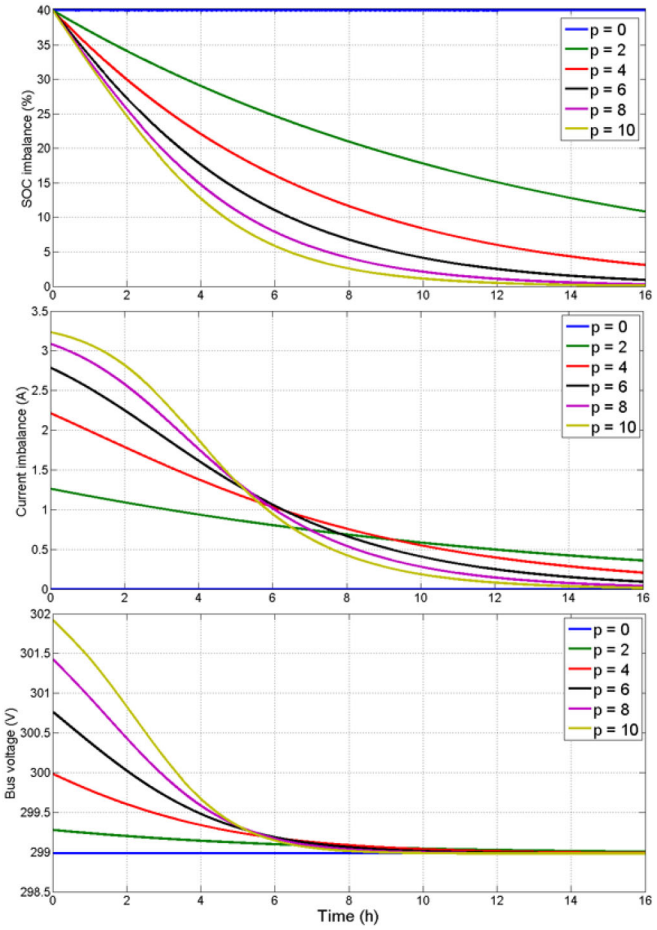

Fig. 5. ESS behavior in discharge mode, for different convergence factors p.

SOC differences will generate unbalanced ESU output currents. Assuming, for sake of simplicity, an ESS composed by two identical ESU with $R_{D1} = R_{D2} = R_D$, and combining (4), (5), (6) and (7), the current imbalance (ΔI) can be determined as (8). The evolution of the SOC difference (ΔSOC) can be expressed as (9), where V_{Bat} is the battery bank terminal voltage.

$$\Delta I = V_{Oref} \left[\frac{1}{R_L} - \frac{2\exp\left(\frac{p\Delta SOC}{2}\right) + \frac{R_D}{R_L}}{R_D + 2R_L \cosh\left(\frac{p\Delta SOC}{2}\right)} \right] \tag{8}$$

$$\Delta SOC = \Delta SOC^0 - \frac{V_O}{V_{Bat} \cdot C_{Bat}} \int \Delta I \cdot dt \tag{9}$$

As ΔI is always positive, during either ESS charge or discharge, the SOC difference will gradually be minimized, converging to zero if all ESU in the storage system are identical. Figure 5 presents SOC difference, output current imbalance and DC bus voltage behavior for a microgrid in stand-alone mode, with $R_D = 2.42\Omega$, $R_L = 90\Omega$, $C_{Bat} = 40Ah$ and $V_{Oref} = 303V$, for different values of p, assuming an initial SOC difference (ΔSOC^0) of 40%. It can be seen that an increase in p promotes a faster SOC equalization, but also a higher initial current imbalance and a reduction in the maximum bus voltage deviation. However, as SOC difference

decreases, the converters output current tends to equalize and the output voltage converge to the original DBS design.

A tradeoff between faster SOC equalization, initial voltage deviation and current imbalance must be defined for each project for the appropriate selection of the convergence factor. In this paper, a convergence factor $p = 6$ was assumed for the remainder of the studies. According to Figure 5, for $p \geq 6$ the DC bus voltage converges to the original DBS value fairly at the same time, however, a lower factor reduces the initial current imbalance. For $p = 6$, the initial current imbalance is below 3A, which, for the experimental prototype, which will be discussed later, allows the converters to operate in this load and SOC imbalance condition without saturating. Therefore, $p = 6$, for the purposes of this paper, presents itself as a good compromise between SOC equalization speed and low interference with DBS design.

It is important to mention that, if the ESU in the storage system do not present identical characteristics, the compensation algorithm will still promote SOC difference minimization, however, depending on the relationship between ESU droop resistance and rated battery bank capacity, it might not be possible to achieve $\Delta I = 0$ and $\Delta SOC = 0$ simultaneously. Considering an example where, an ESS composed of two ESU with identical C_{Bat}, but distinct droop resistances ($R_{D1} \neq R_{D2}$), the current imbalance can be recalculated as (10).

$$\Delta I = \frac{-V_{Oref} \cdot \left[R_{D1} - R_{D2} \exp(p\Delta SOC)\right]}{\left[1 + \frac{R_{D2}\exp(p\Delta SOC)}{R_{D1}} + \frac{R_{D2}}{R_L \exp\left(p\frac{\Delta SOC}{2}\right)}\right] R_L R_{D1}} \tag{10}$$

In equilibrium, the compensation algorithm will manage to ensure current equalization, however, a minimum SOC difference can be expected. Solving (10) so $\Delta I = 0$, results in a minimum ΔSOC which can be expressed by (11).

$$\Delta SOC|_{\Delta I=0} = \Delta SOC_{min} = sgn(i_O) \cdot p^{-1} \ln\left(\frac{R_{D1}}{R_{D2}}\right) \tag{11}$$

It indicates that the unit with the higher droop resistance will handle less power than the other units in the storage system, therefore, its SOC will converge to be the ESS highest in discharge mode, and the lowest in charge mode. Another important aspect of (11), is that increasing the convergence factor p can attenuate the influence of the droop mismatch, inducing a reduction in ΔSOC_{min}.

C. Stability Analysis—Voltage Droop Mode

This section will assess the influence of the SOC balancing algorithm on the microgrid stability during voltage droop mode, where each ESU behaves as a voltage source with virtual series resistance. The following analysis is suitable for non-saturated ESU in both charge and discharge processes. Assuming the diagram shown in Figure 2, considering an ESS with two identical ESU, in order to simplify the analysis, the state space for the boost converters can be expressed as in (12) and (13),

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix} = [A] \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix} + [B] \cdot \begin{bmatrix} \mu_1 \\ \mu_2 \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} i_{O1} \\ i_{O2} \end{bmatrix} = [C] \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix} + [D] \cdot \begin{bmatrix} \mu_1 \\ \mu_2 \end{bmatrix}, \tag{13}$$

where:

$$[A] = \begin{bmatrix} 0 & 0 & -\frac{(1-D_1)}{L_E} \\ 0 & 0 & -\frac{(1-D_2)}{L_E} \\ \frac{(1-D_1)}{2C_O} & \frac{(1-D_2)}{2C_O} & -\frac{1}{2R_L C_O} \end{bmatrix},$$

$$[B] = \begin{bmatrix} \frac{V_O}{L_E} & 0 \\ 0 & \frac{V_O}{L_E} \\ -\frac{I_{L1}}{2C_O} & -\frac{I_{L2}}{2C_O} \end{bmatrix},$$

$$[C] = \begin{bmatrix} (1-D_1) & 0 & 0 \\ 0 & (1-D_2) & 0 \end{bmatrix},$$

$$[D] = \begin{bmatrix} -I_{L1} & 0 \\ 0 & -I_{L2} \end{bmatrix},$$

μ_1 and μ_2 are the converter duty cycles and V_O, I_{L1}, I_{L2}, D_1 and D_2 are steady state values for the bus voltage, inductor currents and duty cycles, respectively. Considering the control diagram in Figure 3, and that the converter operates in voltage droop control, the equation that describes the duty cycle for one of the converters is shown in (14), where V_m is the triangular PWM carrier peak voltage, H_i and H_v are the current and voltage sensor gains, respectively, $C_i(s) = k_{pi} + k_{ii}/s$ is the current loop PI controller and $C_v(s) = k_{pv} + k_{iv}/s$ is the voltage loop PI controller.

$$\mu_j = \frac{1}{V_m}\left\{C_i(s)\left[-H_i i_{Lj} + C_v(s)H_v\left(V_{Oref} - v_o - R_D k_{dj} i_{oj}\right)\right]\right\} \tag{14}$$

Equation (14), can be expressed in matrix form as (15).

$$\begin{bmatrix} \mu_1 \\ \mu_2 \end{bmatrix} = [E] \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix} + [F] \cdot \begin{bmatrix} i_{O1} \\ i_{O2} \end{bmatrix}, \tag{15}$$

where:

$$[E] = \begin{bmatrix} -\frac{C_i(s)H_i}{V_m} & 0 & -\frac{C_i(s)C_v(s)H_v}{V_m} \\ 0 & -\frac{C_i(s)H_i}{V_m} & -\frac{C_i(s)C_v(s)H_v}{V_m} \end{bmatrix},$$

$$[F] = \begin{bmatrix} -\frac{C_i(s)C_v(s)H_v R_D k_{d1}}{V_m} & 0 \\ 0 & -\frac{C_i(s)C_v(s)H_v R_D k_{d2}}{V_m} \end{bmatrix}.$$

Substituting (13) in (15) and the result in (12), the system closed-loop state space can be found and described as (16).

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix} = [A_{CL}]\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_O \end{bmatrix}, \tag{16}$$

where:

$$[A_{CL}] = \left\{[A] + [B](I - [F][D])^{-1}([E] + [F][C])\right\}.$$

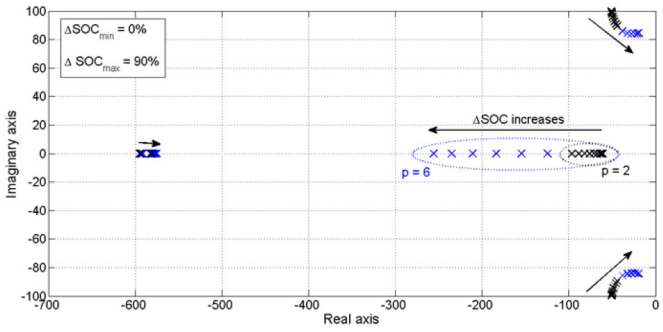

Fig. 6. Dominant poles root locus for the stand-alone microgrid, for $0 \leq \Delta SOC \leq 90\%$ and $p = 2$ (Black markers) and $p = 6$ (Blue markers).

TABLE I
MICROGRID PARAMETERS

Parameter	Value	Parameter	Value
R_D	2.42Ω	H_v	0.01
SOC_1	90%	H_i	0.1
SOC_2	SOC_1-ΔSOC	V_m	3V
R_L	90Ω	k_{pv}	1.5
V_{Oref}	303V	k_{pi}	1.5
V_{Bat}	180V	k_{iv}	510
L_E	750μH	k_{ii}	850
C_O	2mF	$I_{discharge}$	6A
f_{pwm}	17kHz	I_{CMax}	3A

Figure 6 presents the dominant poles root *locus* for the closed loop system, considering the parameters in Table I and a SOC imbalance variation between 0 to 90%. It can be noticed that as SOC imbalance increases a pair of complex poles will move towards the left plan margin, reducing system damping. The convergence factor p influences the depth of variation of the closed loop poles, e.g., for $p = 6$ the complex poles move closer to the right plan than for $p = 2$, meaning that as p increases the system damping decreases even further, for high SOC imbalance. However, in the evaluated conditions, all dominant poles are located at the left-hand side of the complex plan, thus the system will be stable.

III. SIMULATED BEHAVIOR OF THE ENERGY STORAGE MANAGEMENT METHOD

In this section, the behavior of the proposed energy storage management method will be further evaluated through computational simulations, using the software PSIM. The parameters considered for most simulations were the ones described in Table I and $p = 6$.

A. Load Variation Analysis—Two Identical Units

This first simulation analysis will assess the system behavior, considering initial state-of-charge conditions as $SOC_2 = 90\%$ and $SOC_1 = 50\%$, during load variation in stand-alone and connected modes. The simulated Microgrid Thevenin Equivalent Source was implemented as a constant voltage source of 311V with an 1.818Ω series resistor.

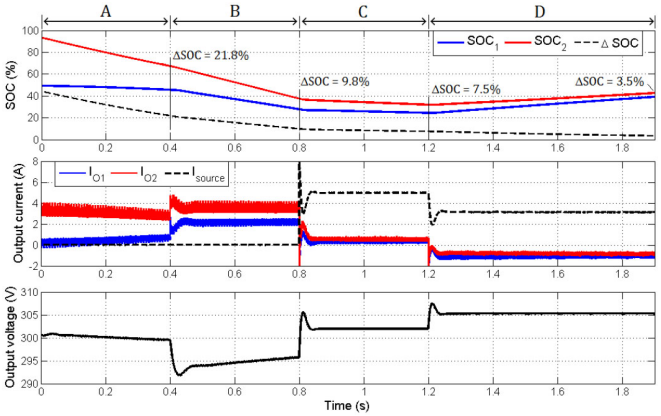

Fig. 7. Simulated results for load variation in a ESS with two identical ESU.

Figure 7 presents the simulation results for the microgrid. The operating conditions seen in the simulation are: A) Stand-alone mode with $R_L = 86\Omega$; B) Stand-alone mode with $R_L = 52\Omega$; C) Connected mode with $R_L = 52\Omega$; D) Connected mode with $R_L = 250\Omega$. The simulation was scaled as $1s = 5h$.

Figure 7 exhibits the instantaneous SOC imbalance at the end of each time interval, showing that the compensation algorithm will promote SOC equalization over the microgrid operation. It can be noticed, that in stand-alone mode, the DC bus voltage varies in accordance to SOC equalization. In this condition, the ESU are responsible for regulating the bus voltage and, due to the balancing algorithm, as the ESU droop resistances are modified it interferes with the system voltage. However, this interference is not enough to jeopardize the power management performed by the microgrid DBS scheme. In situation B, the increase in load power led converter 2 to saturation, what forced a current imbalance reduction, without a proportional SOC difference decrease. As a result, a DC bus voltage drop deeper than expected in normal operation is observed. The bus voltage falls below the DBS limit of 295V, and is gradually restored to its designed value as SOC imbalance is reduced and the compensation factor k_d converges to 1. The microgrid DC bus stays below the DBS limit during 0.2s, reaching a minimum peak of 292V, which represents approximately 1% variation to the DBS window minimum voltage. In connected mode, the microgrid equivalent source is responsible for the DC bus regulation, which reduces the influence of the SOC balancing algorithm to the microgrid operation.

B. Load Variation Analysis—Two Non-Identical Units

In this simulation, the behavior of the management method for two non-identical ESU is evaluated. Converter 1 presents a droop resistance of 3.42Ω, whereas converter 2 maintains the original resistance of 2.42Ω. The units initial state-of-charge were both 65%, since the intention is to highlight the influence of unbalanced droop resistances. Figure 8 presents the results for this simulation. The load variation conditions are the same considered in the previous section.

It can be observed that $\Delta SOC = 0$ is no longer a stable situation, due to droop resistance mismatch. Over the system operation, the units SOC will diverge, however, the difference

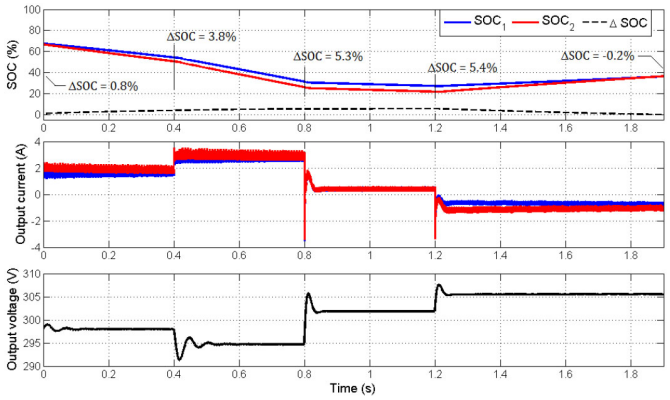

Fig. 8. Simulated results for load variation with two non-identical ESU.

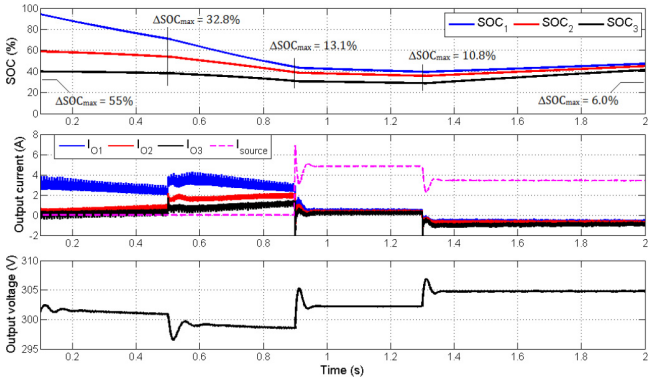

Fig. 9. Simulated results for load variation with three identical units.

stabilizes at approximately 5.4%, which represents a very accurate result, since $\Delta SOC_{min} \approx 5.7\%$, for the simulated conditions, according to (11). It also can be observed that during the charging period ($t > 1.2s$), SOC imbalance is reduced and becomes negative by the end of the simulation, which implies that converter 2, the one with the lower resistance, is absorbing more power than converter 1. As previously discussed, this SOC difference will evolve until it reaches approximately -5.7%.

C. Load Variation Analysis—Three Identical Units

This simulation assesses the behavior of an ESS with higher number of storage units. The load variation conditions are the same considered in previous sections and the initial state-of-charge conditions are $SOC_1 = 95\%$, $SOC_2 = 60\%$ and $SOC_3 = 40\%$. Figure 9 presents the simulation results.

It can be noticed that, over the microgrid operation, the state-of-charge of all three ESU tend to converge to the storage system average, thus, the maximum SOC difference is gradually decreased. The equalization speed is somewhat lower than the observed in a two unit system, which can be explained by the relative reduction in the output power of each unit. Nevertheless, as the SOC balancing algorithm is distributed, as long as the secondary layer is aware of the number of storage units in the ESS, the analysis conducted for an ESS with two units can be extrapolated to a higher set of ESU, meaning that the technique can be employed to storage systems with various distributed storage units.

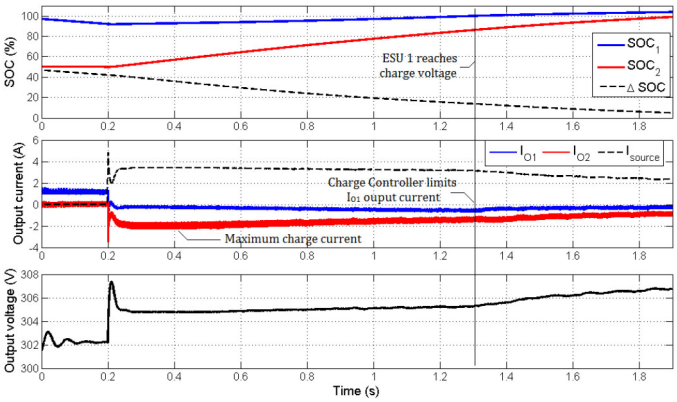

Fig. 10. Simulated results for full charge process.

D. End of Charge Analysis

This simulation evaluates the system behavior during charge mode, as one of the converters reaches full charge condition, i.e., when $SOC \approx 100\%$. The charge behavior of the ESU in a microgrid is shown in Figure 10. Initially the microgrid operates in stand-alone mode, with $R_L = 250\Omega$. In $t = 0.2s$, the microgrid switches to connected mode, and ESU charging begins. The initial state-of-charge conditions in $t = 0.2s$ are $SOC_1 = 90\%$ and $SOC_2 = 50\%$.

Due to the SOC balancing algorithm, converter 2 receives more charge than converter 1. It can be seen that at the beginning of the charge process, converter 2 is saturated by the Charge Controller loop, meaning that the ESU operates with maximum charge current. As SOC difference is reduced, converter 2 charge current is reduced as well, and both converter output currents starts to equalize to an average value. However, in approximately $t = 1.3s$ converter 1 reaches 100% of state-of-charge, meaning also that its correspondent battery bank terminal voltage equals the Charge Controller reference voltage. It indicates that the battery charge method will switch from constant current to constant voltage, thus, the maximum charge current will decrease over time, as the battery bank becomes fully charged, preventing battery overcharge. It can be noticed that, after that event, converter 1 output current starts reducing. As a result the DC bus voltage begins to rise.

IV. Experimental Results

A. Experimental Setup

The proposed Energy Storage Management intends to accomplish charge/discharge control and SOC equalization of distributed ESU in a DBS controlled DC microgrid. The experimental setup used to assess the performance of the proposed system is composed by two 1kW bidirectional boost converters associated in parallel and digitally controlled using a TMS320F28335 DSP by Texas Instruments. The system parameters are described in Table I and the PI controllers were discretized using bilinear transform. Due to limitations of our current testbed, the battery banks were implemented using a power emulator, constituted of a single phase diode rectifier and an one quadrant chopper, and a software real-time battery model, which was implemented directly by the DSP.

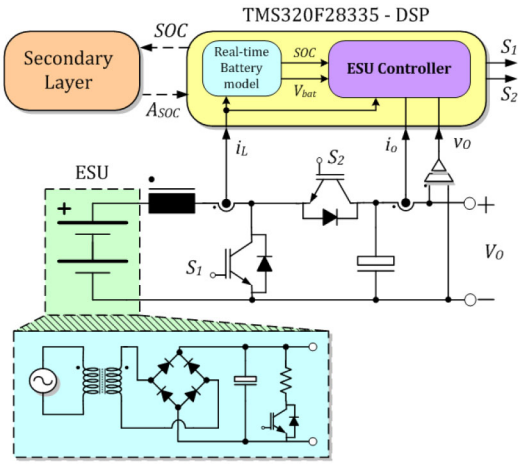

Fig. 11. ESU experimental setup and real-time battery emulator.

Figure 11 shows the diagram of one of the ESU experimental setups. The rectifier is responsible for power supply during ESU discharge and the chopper consumes power during ESU charge, the emulator terminal voltage ranges from 180V to 170V during discharge and 195V in charge mode. The battery emulator measures the converter inductor current and through a real-time battery model, described in [26] and [27], computes the bank state-of-charge and terminal voltage, which are employed in the control loops of the ESU converter.

For the purposes of this paper, the main difference between the experimental setup and a real battery bank, besides the presence of a 120Hz voltage ripple, is that in a real bank, the terminal voltage is dependent on the direction and magnitude of the boost inductor current, whereas in the power emulator, especially in discharge mode, it is steady. This may cause divergences in terms of power saturation limits and system dynamics, although the microgrid dynamics is much faster than the storage devices. Despite these differences, the experimental setup is expected to appropriately represent the storage system.

B. Dynamic Response

The dynamic response evaluation was conducted considering the DC microgrid in connected mode, i.e., a microgrid equivalent power source is attached to the DC bus. This power source was implemented using a 2kW bidirectional buck converter, in voltage droop mode, with droop resistance equal to 1.818Ω and 6.6A current saturation. The ESU initial state-of-charge are $SOC_1 = 55\%$ and $SOC_2 = 95\%$ and the system was tested for convergence factors $p = 6$ and $p = 0$, which represents a situation with no SOC balancing operation. Figure 12 shows the system response for a load step variation from 250Ω to 85.5Ω and Figure 13 presents the response comparison between $p = 0$ and $p = 6$, where i_{O1} and i_{O2} are the boost converter output current as depicted in Figure 2.

The initial condition represents a light load situation for the DC microgrid, therefore the influence of the SOC balancing algorithm on the ESS behavior is not significant, as can be noticed from Figure 13, since DC bus voltage and net ESS current are very similar for different convergence factors. The net

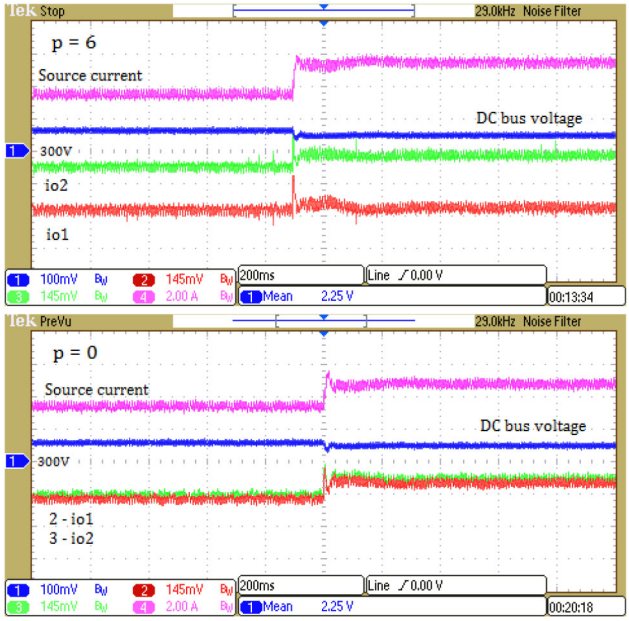

Fig. 12. Load step response $R_L = 250\Omega \rightarrow 85.5\Omega$. Ch1 - 13.7 V/div, Ch2, Ch3 - 1A/Div, Ch4 - 2A/div.

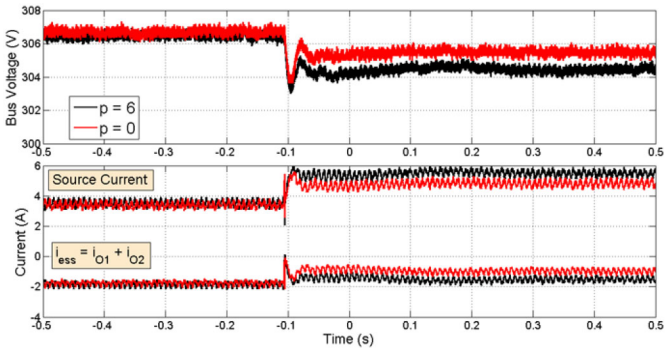

Fig. 13. Comparison between load step responses for $p = 0$ and $p = 6$. $R_L = 250\Omega \rightarrow 85.5\Omega$.

ESS charge power is 547W for $p = 0$ and 563W, for $p = 6$, however, this power is unevenly distributed between the ESU when SOC balancing is active, with converter 1 absorbing 445W while converter 2 consumes 118W. When system load is increased, there is a reduction in the DC bus voltage, forcing the microgrid power source to inject more current in the DC bus and the ESS to decrease its consumed power. In this situation, the system with no SOC balancing showed a reduction in the ESS net consumed power of 248W, while the compensated system presented a 102W power decrease, which is a reflection of the ESS equivalent droop resistance reduction provided by the SOC balancing algorithm. This also promotes steady state bus voltage difference of 0.4V between both systems. SOC compensation did not showed a significant impact on the system dynamic behavior in comparison with the non-compensated system. Figures 14 and 15 present the system response for a step variation from 85.5Ω to 51.6Ω.

As Figures 14 and 15 show, with this further load increase, the microgrid source gets closer to its current saturation level, the non-compensated system ESS reduces its absorbed power

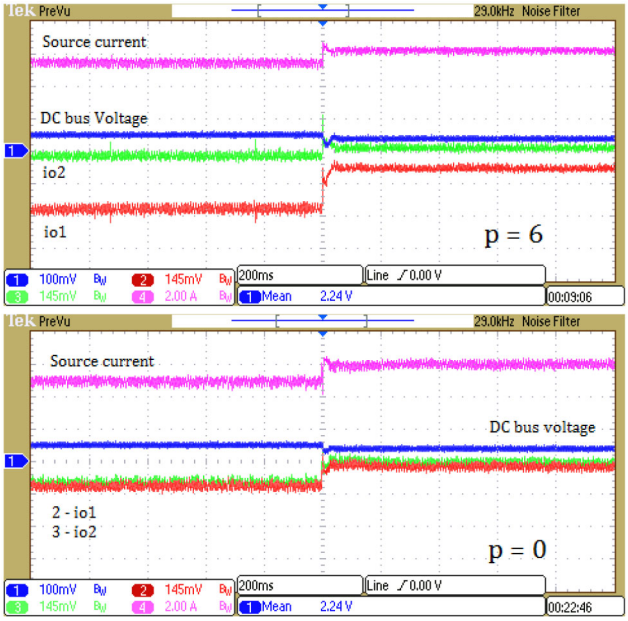

Fig. 14. Load step response $R_L = 85.5\Omega \rightarrow 51.6\Omega$. Ch1 - 13.7 V/div, Ch2, Ch3 - 1A/Div, Ch4 - 2A/div.

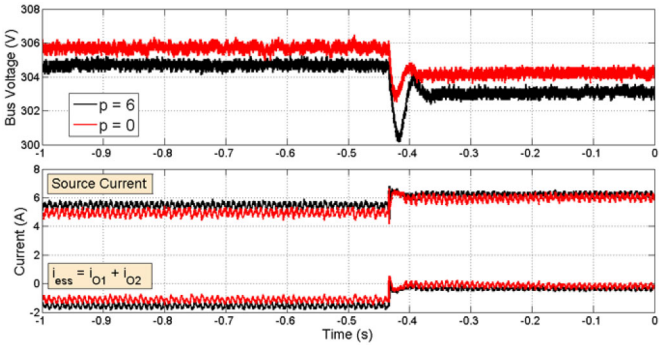

Fig. 15. Comparison between load step responses for $p = 0$ and $p = 6$. $R_L = 85.5\Omega \rightarrow 51.6\Omega$.

to 10W, while the system with SOC compensation consumes 89W. Converter 1 reduces its consumed power from 421W to 127W, while converter 2 shifts from absorbing 40W to injecting 38W, voltage difference between both systems increase to 1V. The compensated system presented a slightly greater voltage undershoot during the step load variation than the non-compensated system. The experiments show that the proposed control diagram can define the ESS power flow properly, according to the DBS design, and that even though the SOC balancing algorithm do interfere with voltage regulation and power exchange between the ESU and the microgrid, this influence is not enough to considerably impact the system behavior and dynamics.

C. SOC Balancing Behavior

This section evaluates the performance of the SOC balancing algorithm. The secondary layer SOC sampling occurred in an 160ms interval. Figure 16 shows the SOC imbalance evolution during a discharge process, considering initial

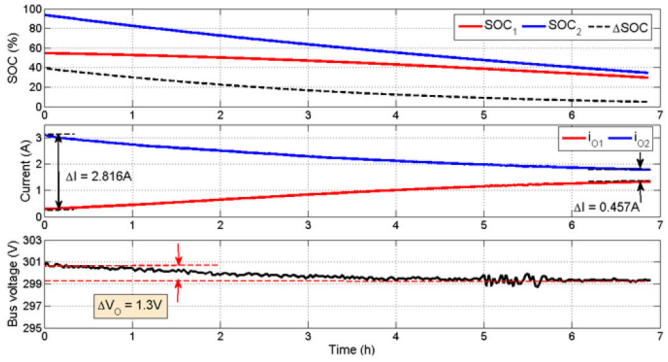

Fig. 16. SOC balancing in discharge mode.

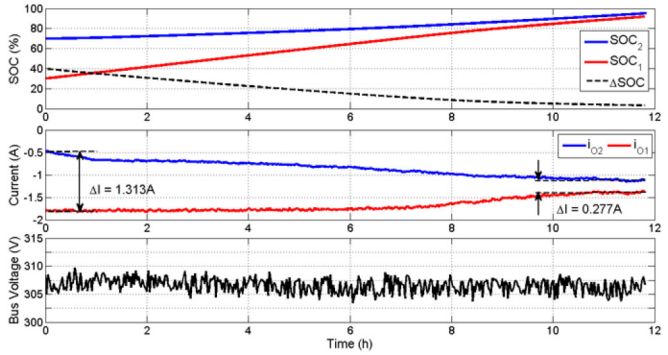

Fig. 17. SOC balancing in charge mode.

states-of-charge $SOC_1 = 55\%$ and $SOC_2 = 95\%$ and load $R_L = 85.5\Omega$, the system operates in stand-alone mode.

Due to the SOC imbalance, converter 2 assumes most of the load current, injecting 3A into the DC bus, against 190mA injected by converter 1. According to the original DBS system design, the DC bus voltage for this load condition would be around 299V, however, since the ESS equivalent droop resistance is lower than the original non-compensated design, the initial bus voltage is 300.6V. As time elapses, SOC difference is decreased. The test was terminated when the state-of-charge of ESU 1 dropped below 30%. At this point SOC difference was 4.85%, current imbalance was reduced to 0.457A and the bus voltage lowered 1.3V, to 299.3V, thus converging to the expected voltage.

The SOC compensation during charge mode is presented in Figure 17. The system operates in connected mode, with load $R_L = 250\Omega$ and initial charge $SOC_1 = 30\%$ and $SOC_2 = 70\%$. As discussed previously, in light load conditions there is no significant difference between the original DBS bus voltage and the compensated system voltage, therefore, along the test the DC bus voltage remained around 306V. Converter 1 absorbs most of the charge power, allowing SOC equalization. As the Charge Controller loop limits the charge inductor current to 3A, independently of SOC compensation, the output current is also limited during charge mode, hence, converter 1 current stays saturated to 1.82A during the first 5h of the test. Converter 2 gradually increases its absorbed power as SOC difference decreases. The test was terminated when ESU 1 SOC reached 95%, leaving a SOC imbalance of

3.26% and current difference of 0.277A. The time needed to reduce the SOC imbalance to a definite level was longer during charge mode than discharge mode. This can be explained due to the fact that charging current is limited to half of the discharge current, which decreases the derivative of SOC compensation.

V. Conclusion

This paper proposed an Energy Storage Management Method to control distributed energy storage units charge/discharge in a DC microgrid, simultaneously promoting SOC equalization between different units, through the employment of DC bus signaling power management and a secondary control layer for SOC balancing. It was discussed that distributed SOC equalization achieved by droop resistance modification will interfere with DC bus voltage deviation, thus altering the static behavior of a DC bus signaling design. The proposed solution only actuates when a SOC imbalance is present, producing an output current imbalance to force charge equalization and the intensity of this current difference is dependent on the level of SOC disparity. A convergence factor can be tuned to promote faster equalization, and compensate the effects of droop resistance mismatch, but, higher convergence factors can further affect voltage deviation over the equalization process, thus a tradeoff between SOC balancing speed and low interference in the DC bus signaling operation must be established to its selection. A communication failure will disable SOC compensation, however, charge/discharge control will remain active, thus such failure will not prevent the microgrid operation, but can lead to non-optimal performance. Experimental results have shown that the system operation can promote power flow control and SOC equalization without producing stability issues. SOC balancing was achieved both in charge and discharge mode.

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